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ATTORNEY DOCKET NO. 10030549-1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Andrew S. Hildebrant, et al.

Serial No.: 10/681,068 Examiner: Frank M. Leiva

Filing Date: October 7, 2003 Group Art Unit: 3714

Title: COST ESTIMATION FOR DEVICE TESTING

COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria VA 22313-1450

TRANSMITTAL OF APPEAL BRIEF

Sir:

Transmitted herewith is the Appeal Brief in this application with respect to the Notice of Appeal filed on September 17, 2007.

The fee for filing this Appeal Brief is (37 CFR 1.17(c)) **$510.00**.

(complete (a) or (b) as applicable)

The proceedings herein are for a patent application and the provisions of 37 CFR 1.136(a) apply.

☐ (a) Applicant petitions for an extension of time under 37 CFR 1.136 (fees: 37 CFR 1.17(a)(1)-(5)) for the total number of months checked below:

☐	one month	$ 120.00
☐	two months	$ 460.00
☐	three months	$1050.00
☐	four months	$1640.00

☐ The extension fee has already been filled in this application.

☒ (b) Applicant believes that no extension of term is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition and fee for extension of time.

Please charge to Deposit Account **08-2623** the sum of $510.00. At any time during the pendency of this application, please charge any fees required or credit any overpayment to Deposit Account **08-2623** pursuant to 37 CFR 1.25.

A duplicate copy of this transmittal letter is enclosed.

☒ I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Date of Deposit: November 19, 2007 **OR**

☐ I hereby certify that this paper is being submitted electronically via EFS-Web to the Patent and Trademark Office on the date shown below.

Date of submission:

Typed Name: Gregory W. Osterloth

Signature: _____

Respectfully submitted,

Andrew S. Hildebrant, et al.

By _____

Gregory W. Osterloth
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Reg. No. 36,232

Date: November 19, 2007

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Appl. No.	:	10/681,068	Confirmation No. : 8619
Appellant	:	Andrew S. Hildebrant, et al.	
Filed	:	October 7, 2003	
TC/A.U.	:	3714	
Examiner	:	Frank M. Leiva	
Docket No.	:	10030549-1	

Mail Stop Appeal Brief – Patents
Commissioner for Patents
P.O. Box 1450
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APPEAL BRIEF

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Mail Stop Appeal Brief – Patents
Commissioner for Patents
P.O. Box 1450
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APPEAL BRIEF

Dear Sir:

This Appeal Brief is submitted in response to the Examiner's Final Office Action dated May 15, 2007.

Appellants filed a Notice of Appeal on September 17, 2007.

Real Party in Interest

The real party in interest is Verigy (Singapore) Pte. Ltd., a Singapore limited liability company.

Related Appeals and Interferences

The rejections of the claims in United States patent application no. 10/666,024 have been appealed to the Board of Patent Appeals and Interferences. The decision on this appeal, when made, could be relevant to the appeal of the rejections of the claims in the instant application.

Status of Claims

Claims 1-17 are pending, all of which stand rejected.

A copy of the claims is attached as a Claims Appendix to this Appeal Brief.

Status of Amendments

No amendments were made to the claims subsequent to final rejection. All amendments have been entered.

Summary of Claimed Subject Matter

In a first embodiment (claim 1) a machine-executable method comprises 1) reading a test file having a plurality of test vectors (p. 5, lines 10-18; FIG. 2, 200), 2) determining a required memory needed to execute the plurality of test vectors (p. 5, line 19 - p. 6, line 13; FIG. 2, 205), and 3) using the required memory to estimate a cost to execute the test vectors (p. 6, lines 14-20; FIG. 2, 210).

In a second embodiment (claim 8), a system (p. 4, lines 3-4; FIG. 1, 100) comprises 1) logic (FIG. 1, 102) to read a test file having a plurality of test vectors (p. 4, lines 5-6; p. 5, lines 10-18) and to determine a required memory needed to execute the plurality of test vectors (p. 4, lines 5-7; p. 5, line 19 - p. 6, line 13), and 2) a billing predictor (p. 4, lines 8-14; p. 6, lines 14-20; FIG. 1, 104), communicatively coupled to the logic, to use the required memory to estimate a cost to execute the test vectors.

In a third embodiment (claim 13), one or more machine-readable mediums have sequences of instructions stored thereon (p. 9, lines 5-10). When executed by a machine, the sequences of instructions cause the machine to perform the following actions: 1) read a test file having a plurality of test vectors (p. 5, lines 10-18; FIG. 2, 200); 2) determine a required memory needed to execute the plurality of test vectors (p. 5, line 19 - p. 6, line 13; FIG. 2, 205); and 3) use the required memory to estimate a cost to execute the test vectors (p. 6, lines 14-20; FIG. 2, 210).

Grounds of Rejection to be Reviewed on Appeal

1. Whether claims 1, 3-7, 12 and 17 should be provisionally rejected under 35 USC 101 as claiming the same invention of claims 1-6 and 10-13 of copending application no. 10/666,024.

2. Whether claims 1-17 should be rejected under 35 USC 112, first paragraph, as failing to comply with the enablement requirement.

3. Whether claims 1-17 should be rejected under 35 USC 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which appellants regard as their invention.

4. Whether claims 1-17 should be rejected under 35 USC 103(a) as being unpatentable over Hughes, Jr. (US Pat. No. 4,493,079) in view of Regelman et al. (US Pat. No. 6,574,626).

Argument

1. Claims 1, 3-7, 12 and 17 should not be provisionally rejected under 35 USC 101 as claiming the same invention of claims 1-6 and 10-13 of copending application no. 10/666,024.

Claim 1 of the instant application recites:

> 1. A machine-executable method comprising:
> reading a test file having a plurality of test vectors;
> determining a required memory needed to execute the plurality of test vectors; and
> using the required memory to estimate a cost to execute the test vectors.

Claim 1 of application no. 10/666,024 recites:

> 1. A method comprising:
> reading a test file including a plurality of test vectors to be applied to a device; and
> determining a required memory needed to execute the plurality of test vectors.

Appellants believe it is clear that the above claims do not recite the "same invention".

Although the Examiner provisionally rejects claims 1, 3-7, 12 and 17 on the basis of "same invention"-type double patenting, the Examiner's sole reason for rejecting these claims is set forth below:

> . . .This is a provisional double patenting rejection since the conflicting claims have not in fact been patented. In addition, the examiner user [*sic;* uses] rationale reasoned from legal precedent that an omission of an element with the consequent loss of its function is deemed obvious. See In re Kuhle, 188 U.S.P.Q.7.
>
> 5/15/2007 Final Office Action, p. 2, sec. 3.

The above reason sounds more like a reason for rejecting claims 1, 3-7, 12 and

17 on the basis of obviousness-type double patenting. However, the Examiner continues to maintain his "same invention"-type double patenting rejection of claims 1, 3-7, 12 and 17.

Appellants believe that a rejection of claims 1, 3-7, 12 and 17, based on "same invention"-type double patenting, is improper for the above reasons. Appellants ask that this rejection be withdrawn.

2. Claims 1-17 should not be rejected under 35 USC 112, first paragraph, as failing to comply with the enablement requirement.

The Examiner states, in part:

> . . .The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. This disclosure fails to state or teach one of ordinary skill in the art how billing predictor 104 "uses the required memory to estimate a cost to execute the test vectors". No working examples disclosing the necessary operation have been provided. Without this disclosure, one skilled in the art cannot practice the invention without undue experimentation because of unknown operation of the billing predictor. Since claims 2-7 are dependent on claim 1, claims 9-12 are dependent on claim 8 & claims 14-17 are dependent on claim 13[,] these claims are also rejected.
>
> 5/15/2007 Final Office Action, pp. 2-3, sec. 5.

Appellants respectfully disagree. Appellants' specification provides various examples of how the billing predictor 104 operates. For example, paragraphs [0017], [0023] and [0024] state:

> [0017] Billing predictor 104 may use the required memory determined 205 by logic 102 to estimate a cost to execute the test vectors. The cost may be estimated by using a billing rate and billing scheme charged for the use of various amounts of memory. The billing rate/scheme may correlate to rates charged by a supplier of test services or may be rates charged to use memory of a tester. Additional factors, such as speed requirements, may also be taken into account when estimating the cost.

[0023] The billing predictor 104 may use various billing rates and schemes that correlate to the configuration of the tester to estimate the cost required to execute the tests. By way of example, in a per pin configuration, billing predictor may use a rate charged for memory to calculate costs to use the required memory for each pin and then total the costs. Correspondingly different calculations may be made for different test environments, such as one memory for tester, or configuration in which all pins on a board are given the same amount of memory but memory can vary between boards.
[0024] The cost estimated 205 by billing predictor 104 may then be displayed to a user. Additional information, such as the test requiring the most memory, may also be provided. The user may use this information to find the lowest cost supplier of test services and/or to reconfigure their tests to meet a test budget.

In response to appellants' above argument, the Examiner asserts:

. . .the applicant points to paragraphs [0017], [0023], and [0024], "stating the use of the memory determined by logic to estimate a cost to execute the test vectors", in which the examiner fails to understand how to exactly estimate the cost on the given information. The examiner still requires undue experimentation to make this statement work. 35 USC § 112 1st paragraph simply requires that applicant to the best of his knowledge, set forth the best mode of operation or practice of his invention at the time of filling his application. Applicant may not conceal the specifics of the preferred invention and disclose to the public only the broad or second best mode of operation.

5/15/2007 Final Office Action, p. 6, sec. 25.

In light of the Examiner's above argument, appellants fail to understand what rejection the Examiner is making. Regarding "enablement", appellants assert that they have fully enabled their "billing predictor 104" by reciting a way in which the billing predictor 104 can perform its function. The way in which the billing predictor 104 can perform its function is recited, at least, in paragraphs [0017], [0023] and [0024] of appellants' specification. Regarding "best mode", appellants are surprised that the Examiner alleges a failure to disclose the best mode, in support of a rejection based on lack of enablement. Enablement and best mode are two separate requirements, and as far as appellants can ascertain, the Examiner has not

specifically rejected appellants' claims for failing to disclose the best mode of their operation.

Appellants believe that a rejection of claims 1-17, based on lack of enablement, is improper for the above reasons. Appellants ask that this rejection be withdrawn.

3. Claims 1-17 should not be rejected under 35 USC 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which appellants regard as their invention.

The Examiner asserts, in part:

> . . .When referring to independent claims 1, 8 & 13, the examiner is unclear as to how the required memory is determined. The applicant uses this claim terminology: "determining a required memory needed to execute the plurality of test vectors."
>
> 5/15/2007 Final Office Action, p. 3, sec. 7.

For claims 1 and 13, the limitation of "determining a required memory needed to execute the plurality of test vectors" is clearly defined by the claims, and is described in the specification of the instant application. For claim 8, the limitation of "logic...to determine a required memory needed to execute the plurality of test vectors" is clearly defined by the claim, and is described in the specification of the instant application. See, for example, paragraphs [0014]-[0016], which state:

> [0014] As shown in FIG. 2, logic 102 may be used to read 200 a test file containing one or more tests to be performed on a device, such as a system-on-a-chip (SOC). Each of the tests may include a plurality of test vectors to be applied to the device under test. Logic 102 may then ***determine 205 a required memory needed to execute the plurality of test vectors. By way of example, the number of test vectors for each test in the test file may be counted and the required memory may be determined to be equal to the number of test vectors required for the test with the highest number of test vectors.***
> [0015] The determination of the required memory may vary depending upon the configuration of the tester. In one embodiment, the tester that is used to

test the device may include a plurality of boards. Each board may include a plurality of pins that may be used to drive inputs and receive outputs from the device under test. Each pin may include its own memory to use during the testing of the device. The memory may be used to store pin specific vector information. In alternate embodiments, memory may not be included on each pin, but may instead be included for each board or other component of the tester, or pooled in a central location and dynamically allocated by a centralized test processor.

[0016] In one embodiment, ***logic 102 may determine 205 an amount of pooled memory required for the tester to execute the test vectors***. In another embodiment, a required memory needed for each board of a tester to execute the test vectors for the board may be determined. By way of example, ***in embodiments having a memory associated with each pin, a required memory needed for each board may be determined by determining the memory requirements for the pin with the highest memory usage***. In a third embodiment, ***logic 102 may determine 205 the required memory needed for each pin to execute the vectors for the pin***. Appropriate determinations 205 for other configurations are also contemplated.

(Emphasis added).

The specification further describes the limitations of "determining a required memory needed to execute the plurality of test vectors" and "logic...to determine a required memory needed to execute the plurality of test vectors" in paragraphs [0018]-[0022], which state:

[0018] FIG. 3 illustrates an exemplary embodiment of a method for determining 205 a required memory that may be used by logic 102. The method begins by determining 305 a first memory requirement for a first pin to execute the test vectors for a first test in the test file. By way of example, ***the first memory requirement may be determined 305 by counting the number of test vectors in the first test for the first pin. The required memory is then set 310 to be equal to the first memory requirement.***

[0019] Another pin of the tester having test vectors in the first test is selected and a second memory requirement for the selected pin to execute the test vectors for the first test is determined 315. ***The second memory requirement may be determined 315 by counting the number of test vectors in the first test for the selected pin. If the second memory requirement exceeds the current value of the required memory 320, the required memory is set 325 equal to the second memory requirement.***

[0020] After 325, or if the second memory requirement does not exceed the current value of the required memory 320, a determination is made as to whether there are more pins 330 having test vectors in the first test to process.

> If there are more pins, processing continues back at 315 for the next pin. Otherwise, a determination is made as to whether there are more tests in the test file 335.
> [0021] If there are more tests, 315-330 are repeated for the next test for each pin having test vectors to execute for the test. After all the tests have been processed, the method ends 340. Thus, it should be appreciated that at the conclusion of the method the required memory is determined to be equal to the memory requirements for the test and pin combination with the highest memory requirements.
> [0022] In alternate embodiments, the required memory may be determined in a manner different from that shown in FIG. 3. The determination 205 may depend upon how available memory is allocated in the tester. For example, in one embodiment, the memory available for a pin may depend on the board where the pin is located. Pins on one board may have the same amount of memory available as other pins on the same board, while the amount of memory available for pins may vary between boards. In this embodiment, ***a required memory may be calculated for each board by determining the memory requirements for the test and pin combination with the highest memory requirements for each board using a method similar to that described in FIG. 3.*** In a second embodiment, memory may be allocated on a per pin basis. In this embodiment, ***a required memory may be determined for each pin.*** Other exemplary embodiments, such as embodiments with one memory available for all the pins of a board, may use corresponding different calculations.
>
> (Emphasis added).

Accordingly, appellants believe that the limitation of "determining a required memory needed to execute the plurality of test vectors" is clear and definite. Appellants also believe that the limitation of "logic...to determine a required memory needed to execute the plurality of test vectors" is clear and definite.

The Examiner further indicates that:

> . . .The examiner is also unclear as to how the cost will be estimated. The applicant states within the Specification that different calculations can be used, but does not state any of the methods as to how the cost will be calculated. The applicant uses this claim terminology: "using the required memory to estimate a cost to execute the test vectors".
>
> 5/15/2007 Final Office Action, p. 3, sec. 7.

Appellants respectfully disagree. For claims 1 and 13, the limitation of "using the required memory to estimate a cost to execute the test vectors" is believed to be clear and definite. This limitation is further described in the specification, as noted below. For claim 8, the limitation of "a billing predictor, communicatively coupled to the logic, to use the required memory to estimate a cost to execute the test vectors" is clear and definite, and is also further described in the specification. See, for example, paragraphs [0017], [0023] and [0024], which state:

> [0017] Billing predictor 104 may use the required memory determined 205 by logic 102 to estimate a cost to execute the test vectors. The cost may be estimated ***by using a billing rate and billing scheme charged for the use of various amounts of memory.*** The billing rate/scheme may correlate to rates charged by a supplier of test services or may be rates charged to use memory of a tester. Additional factors, such as speed requirements, may also be taken into account when estimating the cost.
>
> [0023] The billing predictor 104 may use various billing rates and schemes that correlate to the configuration of the tester to estimate the cost required to execute the tests. ***By way of example, in a per pin configuration, billing predictor may use a rate charged for memory to calculate costs to use the required memory for each pin and then total the costs.*** Correspondingly different calculations may be made for different test environments, such as one memory for tester, or configuration in which all pins on a board are given the same amount of memory but memory can vary between boards.
> [0024] The cost estimated 205 by billing predictor 104 may then be displayed to a user. Additional information, such as the test requiring the most memory, may also be provided. The user may use this information to find the lowest cost supplier of test services and/or to reconfigure their tests to meet a test budget.
>
> (Emphasis added).

Accordingly, appellants believe that the limitation of "using the required memory to estimate a cost to execute the test vectors" is clear and definite. Appellants also believe that the limitation of "a billing predictor, communicatively coupled to the logic, to use the required memory to estimate a cost to execute the test vectors" is clear and definite.

Appellants believe that a rejection of claims 1-17, based on indefiniteness, is improper for the above reasons. Appellants ask that this rejection be withdrawn.

4. Claims 1-17 should not be rejected under 35 USC 103(a) as being unpatentable over Hughes, Jr. (US Pat. No. 4,493,079; hereinafter "Hughes") in view of Regelman et al. (US Pat. No. 6,574,626; hereinafter "Regelman").

A. Claims 1, 2, 5, 8, 9 & 12-14:

With respect to claim 1, the Examiner admits that:

> . . .*Hughes, Jr. does not disclose determining a required memory needed to execute the plurality of test vectors and using the required memory to estimate a cost to execute the test vectors.*
>
> 5/15/2007 Final Office Action, p. 4, sec. 10.

Appellants agree. However, and also with respect to claim 1, the Examiner asserts that:

> . . .Regelman et al. teaches determining a required memory needed to execute the plurality of test vectors (column 2 lines 31-34); and using the required memory to estimate a cost to execute the test vectors (*the examiner views this limitation as since the required memory is determined, the estimated cost can be determined. In addition, the estimated cost is determined based on how much memory is required. Since the memory is costly then we the public would know that the estimated cost will also be costly.)* It would have been obvious to one of ordinary skill in the art at the time the invention was made to include determining a required memory and estimating the cost, as disclosed by Regelman, incorporated into Hughes, Jr. so that cost effective memory can be used to satisfy the problem.
>
> 5/15/2007 Final Office Action, p. 4, sec. 10.

Appellants respectfully disagree. Regelman's column 2, lines 31-35, state:

> ...As test programs increase in size, a natural solution is to merely increase the amount of embedded SRAM in order to accommodate the entire test program. SRAM, however, is expensive.

The above except merely conveys the general principles that 1) memory is expensive, and 2) as the size of a test program increases, more memory is needed to accommodate the test program. However, the above excerpt does not teach or suggest that a "machine-executable method" should determine the "required memory" needed to execute a plurality of test vectors, or that the required memory should be used to estimate a "cost to execute the test vectors".

As taught in paragraph [0012] of appellants' specification, determining the memory required to execute a plurality of test vectors, and then using the required memory to estimate the cost of executing the test vectors, can enable a user to meet a test budget or choose an appropriate supplier of test services. Regelman does not discuss any such need for (or advantages of) estimating the cost to execute a plurality of test vectors. In fact, Regelman's disclosure says nothing about estimating the cost to execute a plurality of test vectors. Rather, Regelman's disclosure is directed to methods and apparatus for administering extended memory (see, e.g., Regelman's Title). That is, Regelman starts with the premise that larger test programs require more memory "to accommodate the entire test program" (col. 2, lines 31-34). Then, *and instead of* indicating that it would be useful to estimate the cost to execute a plurality of test vectors, Regelman describes a method for 1) distributing a test program between primary and secondary memories, and 2) executing the test program by executing a pattern stored in the primary memory. See, Regelman, col. 2, lines 51-59. Because Regelman's method "permits efficient and cost effective use of DRAM in conjunction with SRAM to achieve optimal program storage and performance" (col. 3, lines 37-39), Regelman apparently has no need to estimate the actual cost of executing a plurality of test vectors (and is thus silent regarding same).

Claim 1 is believed to be allowable for at least the above reasons.

Claims 2 & 5 are believed to be allowable, at least, because they depend from claim 1.

Claim 8 is believed to be allowable, at least, for reasons similar to why claim 1 is believed to be allowable.

Claims 9 & 12 are believed to be allowable, at least, because they depend from claim 8.

Claim 13 is believed to be allowable, at least, for reasons similar to why claim 1 is believed to be allowable.

Claim 14 is believed to be allowable, at least, because it depends from claim 13.

B. Claims 3, 4, 10, 11, 15 & 16:

Claims 3 & 4 are believed to be allowable, in one respect, because they depend from claim 1. Claims 3 & 4 are also believed to be separately allowable, because they respectively recite "determining a required memory needed for each of a plurality of boards of a tester to execute the test vectors for the board" and "determining a required memory needed for each of a plurality of pins of a tester to execute the test vectors for the pin".

In support of the rejections of these claims, the Examiner asserts that Regelman discloses determining the required memory needed for each of a plurality of boards and pins in col. 4, lines 5-20. Appellants disagree. Although Regelman teaches that a test system may comprise "test resources", "test points", and "channels" having pin electronics, Regelman does not indicate that the required memory needed to execute a plurality of test vectors should be determined on a per board or per pin basis.

Claims 10 & 11 are believed to be allowable, at least, for reasons similar to why

claims 3 & 4 are believed to be allowable.

Claims 15 & 16 are believed to be allowable, at least, for reasons similar to why claims 3 & 4 are believed to be allowable.

C. Claims 6, 7 & 17:

Claims 6 & 7 are believed to be allowable, in one respect, because they depend from claim 1. Claim 6 is also believed to be separately allowable, because it recites a specific method for determining the required memory for executing a plurality of test vectors, which method is not taught by Hughes or Regelman.

The Examiner asserts that the method steps set forth in claim 6 are taught by Regelman in col. 20, lines 50-54. However, these lines state:

> . . .In the example, there is insufficient room in the primary memory 20 to merely add the smaller test pattern #4 808. Accordingly, the memory management software allocates space and then overwrites beginning at a primary memory location designated as the first memory location of test pattern #2 804.

Regelman, col. 20, lines 49-54.

Appellants can find nothing in the above excerpt which is pertinent to the method for determining a required memory recited in claim 6, in which the method comprises:

> determining a first memory requirement needed for a first pin of a tester to execute the test vectors for a first test in the test file;
> setting the required memory equal to the first memory requirement; and
> for each additional pin of the tester,
> determining a second memory requirement needed for the additional pin to execute the test vectors for the first test; and
> if the second memory requirement is greater than the first memory requirement, setting the required memory equal to the second memory requirement.

Claim 6 is therefore believed to be allowable for the above additional reason.

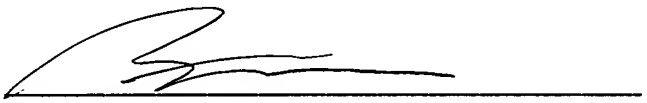
Claim 7 is believed to be allowable for the additional reason that it depends from claim 6.

Claim 17 is believed to be allowable, at least, for reasons similar to why claim 6 is believed to be allowable.

5. Conclusion

In summary, the art of record does not teach nor suggest the subject matter of appellant's claims 1-17. These claims are therefore believed to be allowable.

Respectfully submitted,
HOLLAND & HART, LLP

By: 

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Claims Appendix

1. A machine-executable method comprising:

reading a test file having a plurality of test vectors;

determining a required memory needed to execute the plurality of test vectors; and

using the required memory to estimate a cost to execute the test vectors.

2. The method of claim 1, further comprising receiving a billing scheme and wherein using the required memory to estimate a cost includes using the billing scheme to estimate the cost to execute the test vectors.

3. The method of claim 1, wherein determining a required memory comprises determining a required memory needed for each of a plurality of boards of a tester to execute the test vectors for the board.

4. The method of claim 1, wherein determining a required memory comprises determining a required memory needed for each of a plurality of pins of a tester to execute the test vectors for the pin.

5. The method of claim 1, wherein determining a required memory comprises counting the number of test vectors for each of one or more tests in the test file.

6. The method of claim 1, wherein determining a required memory comprises:

determining a first memory requirement needed for a first pin of a tester to execute the test vectors for a first test in the test file;

setting the required memory equal to the first memory requirement; and

for each additional pin of the tester,

determining a second memory requirement needed for the additional pin to execute the test vectors for the first test; and

if the second memory requirement is greater than the first memory requirement, setting the required memory equal to the second memory requirement.

7. The method of claim 6, further comprising for each additional test in the test file:

for each pin of the tester, determining a third memory requirement for the pin to execute the test vectors for the additional test; and setting the required memory equal to the third memory requirement if the third memory requirement is greater than the required memory.

8. A system comprising:

logic to read a test file having a plurality of test vectors and to determine a required memory needed to execute the plurality of test vectors; and

a billing predictor, communicatively coupled to the logic, to use the required memory to estimate a cost to execute the test vectors.

9. The system of claim 8, further comprising a user interface to display the cost to a user.

10. The system of claim 8, wherein the tester includes a plurality of boards, and wherein the logic is to determine a required memory needed for each board of a tester to execute the test vectors for the board.

11. The system of claim 8, wherein the tester includes a plurality of boards, each board including a plurality of pins; and wherein the logic is to determine a required memory needed for each pin to execute the test vectors for the pin.

12. The system of claim 8, wherein the logic is to determine the required memory by counting the number of test vectors for each test in the test file.

13. One or more machine-readable mediums having stored thereon sequences of instructions, which, when executed by a machine, cause the machine to perform the actions:

reading a test file having a plurality of test vectors;

determining a required memory needed to execute the plurality of test vectors; and

using the required memory to estimate a cost to execute the test vectors.

14. The machine-readable mediums of claim 13, further comprising instructions, which when executed by the machine, cause the machine to perform the actions of receiving a billing scheme; and wherein the instructions for using the required memory to estimate a cost include instructions, which when executed by the machine, cause the machine to perform the actions of using the billing scheme to estimate the cost to execute the test vectors.

15. The machine-readable mediums of claim 13, wherein the instructions for determining a required memory comprise instructions, which when executed by the machine, cause the machine to perform the actions of determining a required memory needed for each of a plurality of boards of a tester to execute the test vectors for the board.

16. The machine-readable mediums of claim 13, wherein the instructions for determining a required memory comprise instructions, which when executed by the machine, cause the machine to perform the actions of determining a required memory needed for each of a plurality of pins of a tester to execute the test vectors for the pin.

17. The machine-readable mediums of claim 13, wherein the instructions for determining a required memory comprise instructions, which when executed by the machine, cause the machine to perform the actions:

determining a first memory requirement needed for a first pin of a tester to

execute the test vectors for a first test in the test file;

setting the required memory equal to the first memory requirement; and

for each additional pin of the tester,

determining a second memory requirement needed for the additional pin to execute the test vectors for the first test; and

if the second memory requirement is greater than the first memory requirement, setting the required memory equal to the second memory requirement.

Evidence Appendix

None.

Related Proceedings Appendix

None.